1) The SOP expression for c_8 in a carry-lookahead adder is

$$c_8 = g_7 + p_7g_6 + p_7p_6g_5 + p_7p_6p_5g_4 + p_7p_6p_5p_4g_3 + p_7p_6p_5p_4p_3g_2 + \\ + p_7p_6p_5p_4p_3p_2g_1 + p_7p_6p_5p_4p_3p_2p_1g_0 + p_7p_6p_5p_4p_3p_2p_1p_0c_0$$

Show how to implement this expression if only gates with at most 4 inputs can be used. Rewrite the expression for c_8 using parentheses to show the associated grouping of inputs. Sketch and label the corresponding circuit and determine its cost. The first priority for optimization is to keep the longest delay from any of the inputs to the c_8 output as short as possible. The second priority is to minimize the cost of the circuit. Compare the longest delay from input to output and the cost of your circuit to the cost and delay of a direct SOP implementation (without gate input constraints) for c_8.

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